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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,699	12/01/2003	Francois X. Prinz	24317/82501	2551

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EXAMINER	
BEHM, HARRY RAYMOND	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,699	PRINZ ET AL.	
	Examiner	Art Unit	
	Harry Behm	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,8-14 and 16* is/are rejected.

7)☒ Claim(s) *2,5,7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in Fig. 2, the input REF 110 to comparator 158 is not different than the input to comparator 154. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: Paragraph 35 lines 2 and 5 refer to oscillator 108 in Fig. 2. There is no reference to 108 in Fig. 2.

3. Appropriate correction is required.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The following title is suggested: Digital control of switching voltage regulators operated in discontinuous mode with multiple feedback error comparators providing information on the rate of change of the output voltage used to reduce output voltage droop.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 3, 4, 6, 8 -14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Sutardja (US 20040239300).

8. With respect to Claim 1, Sutardja discloses a digital control system (Fig. 1 10) for voltage converters, comprising: an oscillator (Fig. 2 122) that issues a pulse; a duty cycle generator (Fig. 27 950), wherein the pulse is used to load a numerical value (Fig. 27 "counter limit") stored in a memory of the system into the duty cycle generator (Fig. 27 950); a digital counter (Fig. 27 958) that stores and alters a duty cycle (Fig. 27 "counter limit"); a first comparator (para 73 line 2 "regulated output is sensed and compared to a reference") that determines how the duty cycle (para 73 line 8 "estimated duty cycle") must be modified; and an algorithm generator (Fig. 2 102) producing an algorithm that determines the rate of change of the duty cycle (Fig. 27 "counter limit").

9. With respect to Claim 3, Sutardja discloses the system of claim 2 further comprising a second comparator (Fig. 10 456) having a reference (Fig. 10 454) different than the first comparator (Fig. 10 456).

10. With respect to Claim 4, Sutardja discloses a method for producing a desired output voltage (Fig. 1 Vout) comprising: storing in memory, an indication (para 73 line 9 "counter limit") of a pulse duty cycle needed for a varying load; monitoring (Fig. 3 150) the load; altering the stored duty cycle (para 73 line 8 "estimated duty cycle") at a first frequency to produce the desired output voltage (Fig. 1 Vout) based upon the indication (para 73 line 10 "function of a clock signal and counter limit"); and if a change in the load (Fig. 1 12) is detected (para

73 line 16 "input greater than a predetermined current"), changing the frequency of alteration of the duty cycle (Fig. 3 158).

11. With respect to Claim 6, Sutardja discloses the method of claim 4 wherein monitoring the load comprises usage of two or more comparators (Fig. 10 456).

12. With respect to Claim 8, Sutardja discloses the method of claim 6, wherein the two or more comparators (Fig. 10 456) each have a different reference (Fig. 10 454).

13. With respect to Claim 9, Sutardja discloses a voltage converter that produces an output voltage (Fig. 1 Vout), comprising: a digital controller (Fig. 2 102) that controls the output voltage (Fig. 1 Vout) of analog circuitry (Fig. 1 114a); a numerical value (Fig 27 "counter limit") stored in a memory of the converter; a duty cycle generator (Fig. 27 950) that utilizes the numerical value (Fig 27 "counter limit") to alter the duty cycle (para 73 line 9 "estimated duty cycle") of the analog circuitry; a first comparator (para 73 line 2 "regulated output is sensed and compared to a reference") that compares the output voltage to a reference voltage at a first rate; and a second comparator (Fig. 10 456) that compares the output voltage to the reference voltage (Fig. 10 454) at a second rate, wherein the numerical value (Fig 27 "counter limit") is updated based upon a comparison at the first or second rate

(para 146 line 6-7 "control the count of the nominal duty cycle based on the outputs of the comparators").

14. With respect to Claim 10, Sutardja discloses the voltage converter of claim 9 further comprising an algorithm generator (Fig. 31B 1008) that selects the speed (Fig. 27 clock) that the numerical value (Fig 27 "counter limit") is updated.

15. With respect to Claim 11, Sutardja discloses the voltage converter of claim 9 wherein the digital controller (Fig. 2 102) selects either the first or second rate (para 146 line 6-7 "control the count of the nominal duty cycle based on the outputs of the comparators").

16. With respect to Claim 12, Sutardja discloses the voltage converter of claim 9 wherein when either comparator (Fig. 10 456) detects that the output voltage (Fig. 1 Vout) is higher than the reference voltage (Fig. 10 454) it decreases the duty cycle (Fig. 27 950).

17. With respect to Claim 13, Sutardja discloses the voltage converter of claim 9 wherein when either comparator (Fig. 10 456) detects that the output voltage (Fig. 1 Vout) is lower than the reference voltage (Fig. 10 454) it increases the duty cycle (Fig. 27 950).

18. With respect to Claim 14, Sutardja discloses the voltage converter of claim 9 wherein the numerical value (Fig. 27 "counter limit") is stored in an up-down counter (Fig. 27 958) in the memory, and wherein if either comparator (Fig. 10 456) detects that the output (Fig. 1 Vout) is

lower than the reference voltage (Fig. 10 454) it switches the up-down counter in up mode (Fig. 27 Up*), and if the reference voltage is lower, it switches the up-down counter in down (Fig. 27 Down*) mode.

19. With respect to Claim 16, Sutardja discloses a digital controller of a voltage regulator, comprising: an up/down counter (Fig. 27 958) that stores a numerical value (Fig. 27 "counter limit") used to alter a duty cycle of the controller driving a transistor/switch; a duty cycle generator (Fig. 27 950) that utilizes the numerical value (Fig. 27 "counter limit") to alter the duty cycle (Fig. 27 UD); and an algorithm generator (Fig. 2 102) that produces an algorithm that alters the rate of change of the duty cycle (Fig. 27 UD).

Allowable Subject Matter

20. Claims 2, 5, 7, and 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is an examiner's statement of reasons for allowance: Claim 2 is allowable because the prior art does not suggest using the comparator to retard switching. Claim 5 is allowable because the prior art does not suggest changing the frequency of updating the digital counter. Claim 7 is allowable because the prior art does not suggest how to minimize dip in the output voltage by changing the frequency of

the digital counter. Claim 15 is allowable because the prior art does not suggest detecting the rate of change of an output voltage over time.

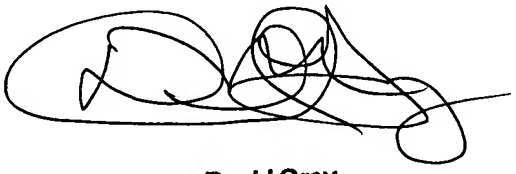
22. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached during business hours EST.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on 571-272-2119. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Gray
Primary Examiner

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